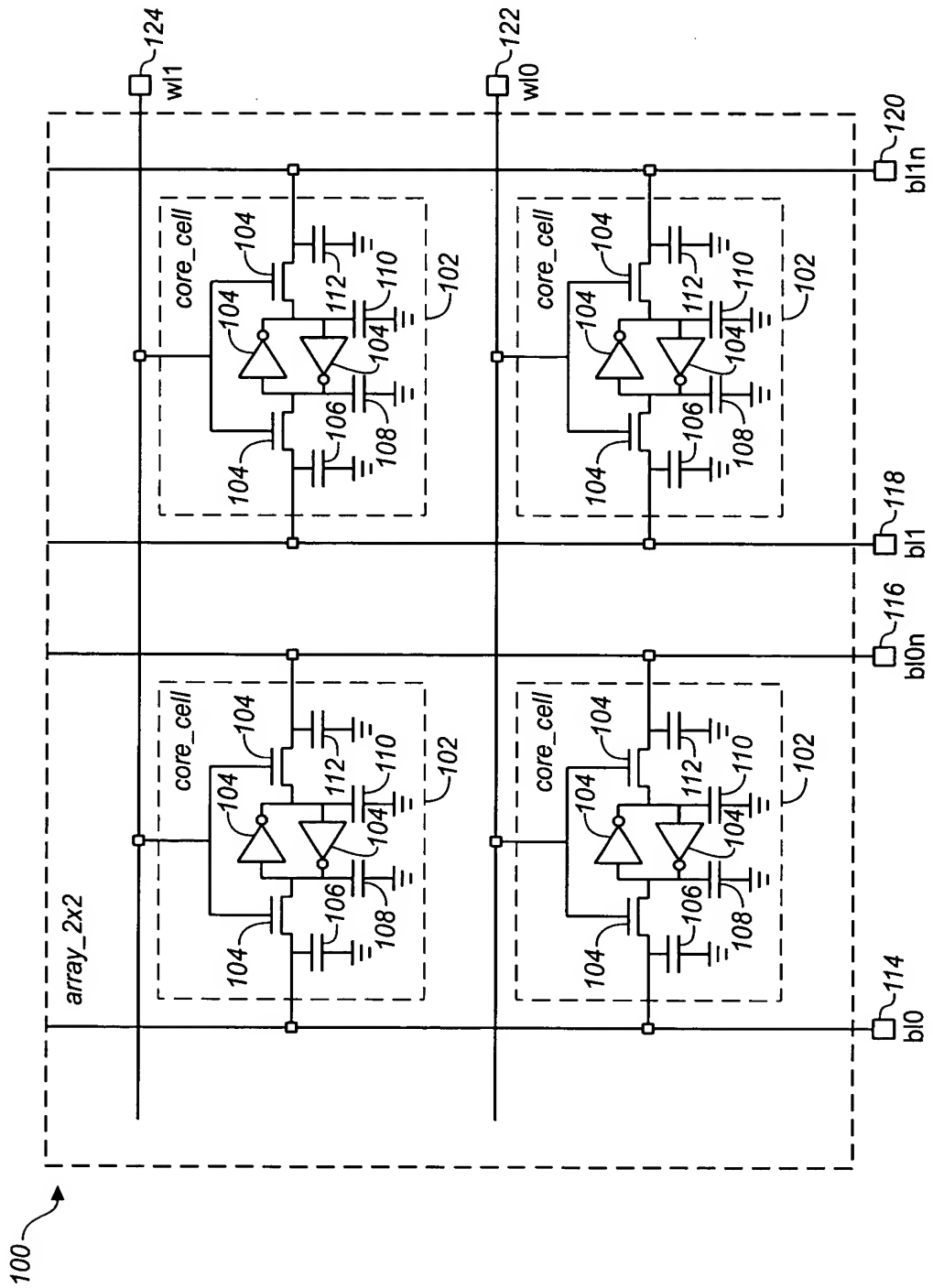

FIG._1
(PRIOR ART)

```
.subckt array2x2 wl0 wl1 bl0 bl0n bl1 bl1n
X00 wl0 bl0 bl0n core_cell
X01 wl0 bl1 bl1n core_cell
X10 wl1 bl0 bl0n core_cell
X11 wl1 bl1 bl1n core_cell
.ends

.subckt core_cell wl bla blan
t0 bla  wl n0 vss nm
t1 blan wl n1 vss nm
t2 n1 n0 vdd vdd pm
t3 n1 n0 vss vss nm
t4 n0 n1 vdd vdd pm
t5 n0 n1 vss vss nm
cp1 bla vss
cp2 blan vss
cp3 wl vss
cp4 n0 vss
cp5 n1 vss
.ends
```

202

204

200

FIG._2 *(PRIOR ART)*

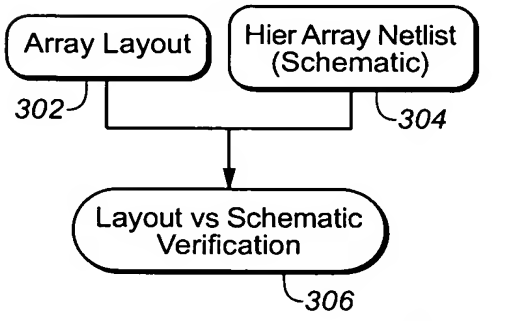

FIG._3
(PRIOR ART)

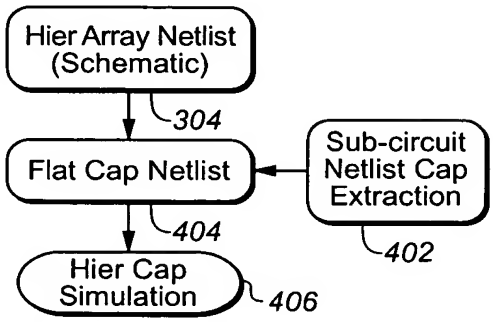

FIG._4
(PRIOR ART)

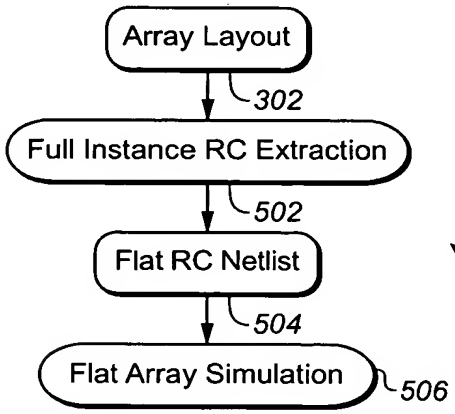

FIG._5
(PRIOR ART)

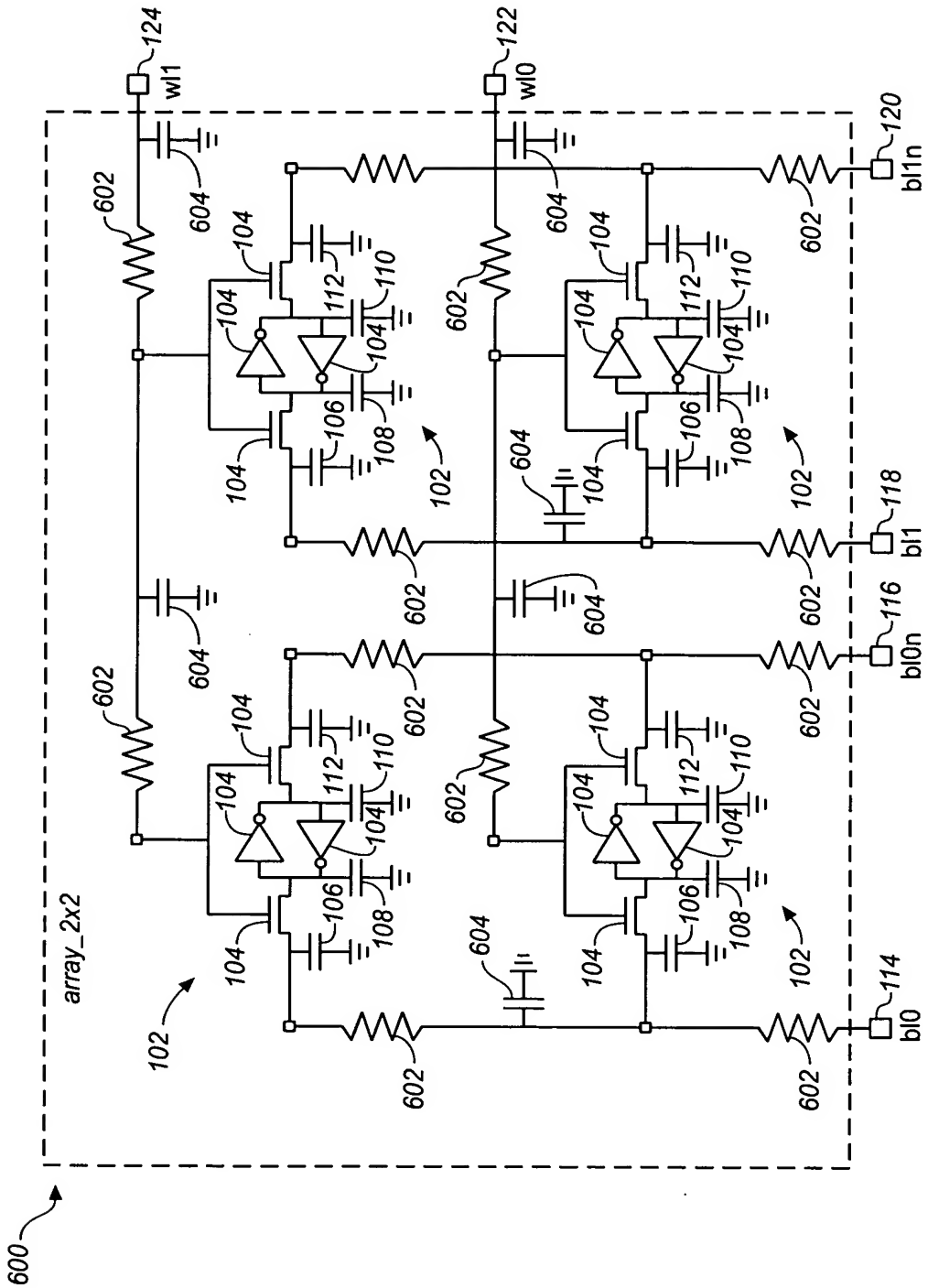

FIG._6
(PRIOR ART)

```
.subckt array2x2 wl0 wl1 bl0 bl0n bl1 bl1n
t00 n2 n1 n4 vss nm
t01 n3 n1 n5 vss nm
t02 n5 n4 vdd vdd pm
t03 n5 n4 vss vss nm
t04 n4 n5 vdd vdd pm
t05 n4 n5 vss vss nm
t06 n7 n6 n9 vss nm
t07 n8 n6 n10 vss nm
t08 n10 n9 vdd vdd pm
t09 n10 n9 vss vss nm
t10 n9 n10 vdd vdd pm
t11 n9 n10 vss vss nm
t12 n12 n11 n14 vss nm
t13 n13 n11 n15 vss nm
t14 n15 n14 vdd vdd pm
t15 n15 n14 vss vss nm
t16 n14 n15 vdd vdd pm
t17 n14 n15 vss vss nm
t18 n17 n16 n19 vss nm
t19 n18 n16 n20 vss nm
t20 n20 n19 vdd vdd pm
t21 n20 n19 vss vss nm
t22 n19 n20 vdd vdd pm
t23 n19 n20 vss vss nm
r00 wl0 n1
c00 n1 vss
r01 n1 n11
c01 n11 vss
r02 wl1 n6
c02 n6 vss
...
.ends
```

700

FIG._7 (PRIOR ART)

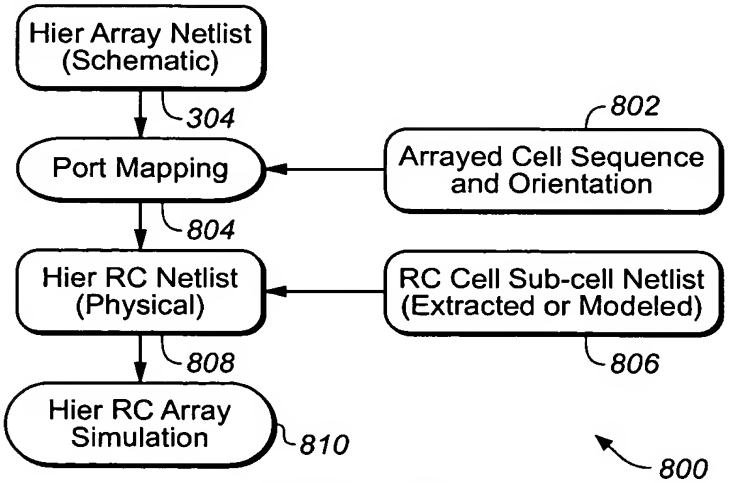

FIG._8

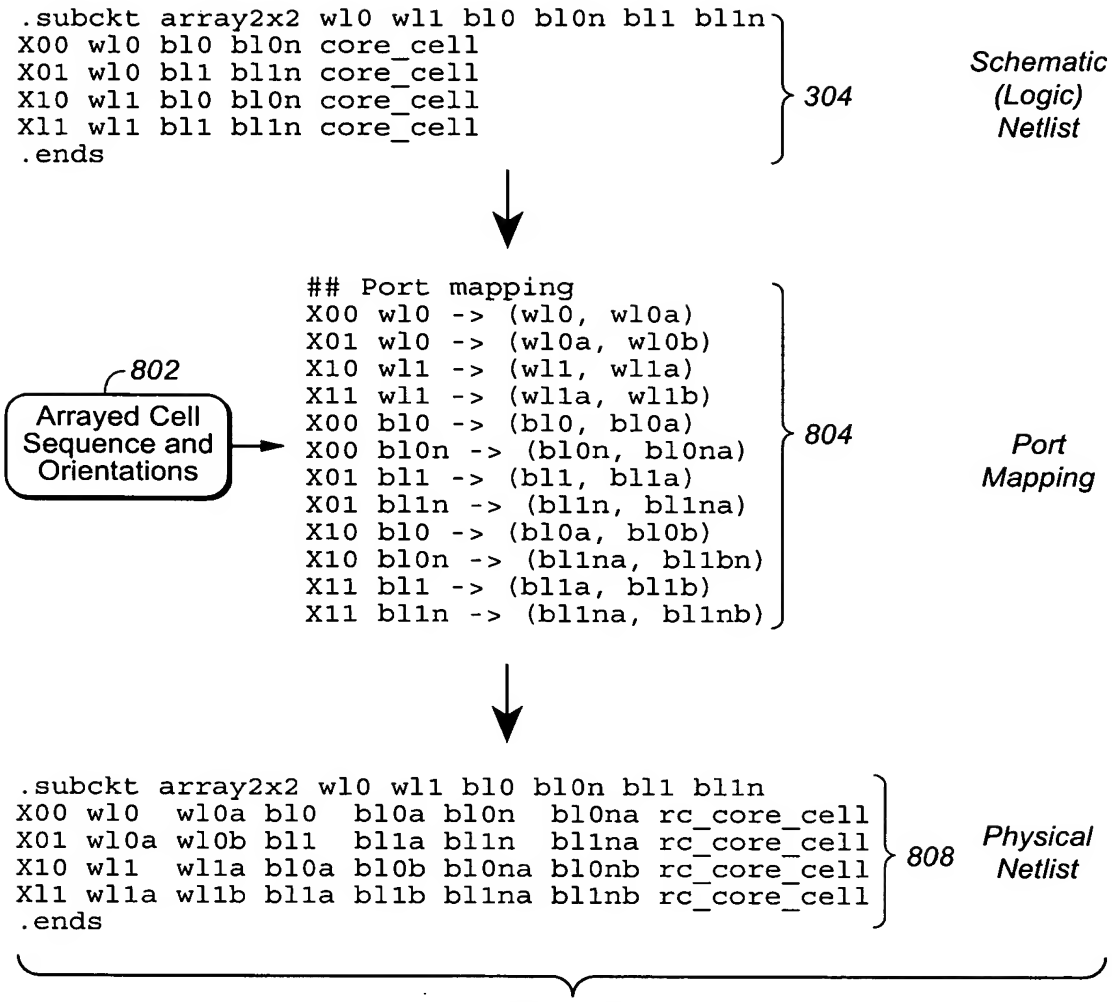
.subckt array2x2 wl0 wl1 bl0 bl0n bl1 bl1n
X00 wl0 bl0 bl0n core_cell
X01 wl0 bl1 bl1n core_cell
X10 wl1 bl0 bl0n core_cell
X11 wl1 bl1 bl1n core_cell
.ends
304
Schematic (Logic) Netlist
802
Arrayed Cell Sequence and Orientations
Port mapping
X00 wl0 -> (wl0, wl0a)
X01 wl0 -> (wl0a, wl0b)
X10 wl1 -> (wl1, wl1a)
X11 wl1 -> (wl1a, wl1b)
X00 bl0 -> (bl0, bl0a)
X00 bl0n -> (bl0n, bl0na)
X01 bl1 -> (bl1, bl1a)
X01 bl1n -> (bl1n, bl1na)
X10 bl0 -> (bl0a, bl0b)
X10 bl0n -> (bl1na, bl1bn)
X11 bl1 -> (bl1a, bl1b)
X11 bl1n -> (bl1na, bl1nb)
804
Port Mapping
.subckt array2x2 wl0 wl1 bl0 bl0n bl1 bl1n
X00 wl0 wl0a bl0 bl0a bl0n bl0na rc_core_cell
X01 wl0a wl0b bl1 bl1a bl1n bl1na rc_core_cell
X10 wl1 wl1a bl0a bl0b bl0na bl0nb rc_core_cell
X11 wl1a wl1b bl1a bl1b bl1na bl1nb rc_core_cell
.ends
808
Physical Netlist

FIG._9

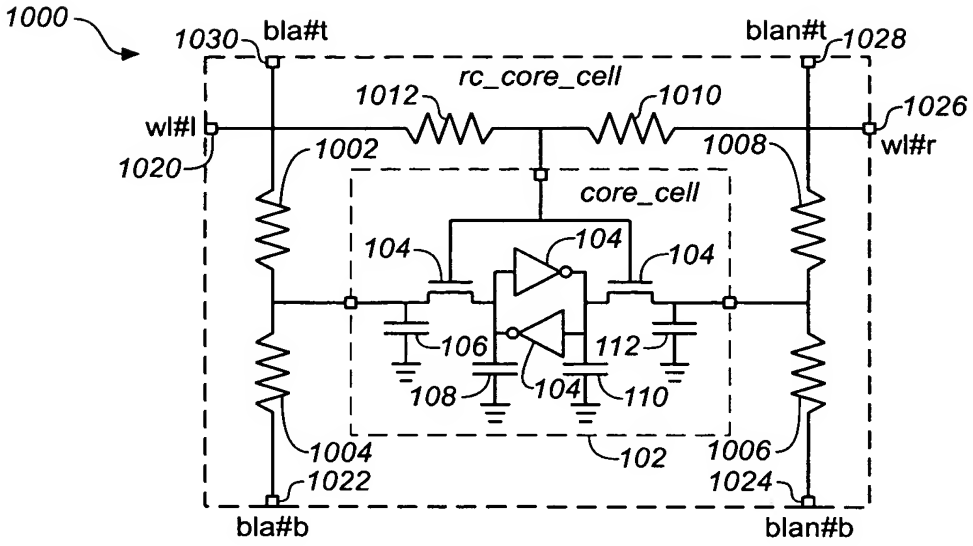

FIG._10

```
.subckt rc_core_cell wl#r wl#1 bla#b bla#t blan#b blan#t
r1 wl#r wl
r2 wl#1 wl
r3 bla#b bla
r4 bla#t bla
r5 blan#b blan
r6 blan#t blan
xl wl bla blan core_cell
.ends
```

1100

FIG._11

```
.subckt array2x2 wl0 wl1 bl0 bl0n bl1 bl1n
X00 wl0  wl0a bl0  bl0a bl0n  bl0na rc_core_cell
X01 wl0a wl0b bl1  bl1a bl1n  bl1na rc_core_cell
X10 wl1  wl1a bl0a bl0b bl0na bl0nb rc_core_cell
X11 wl1a wl1b bl1a bl1b bl1na bl1nb rc_core_cell
.ends
```

1300

FIG._13

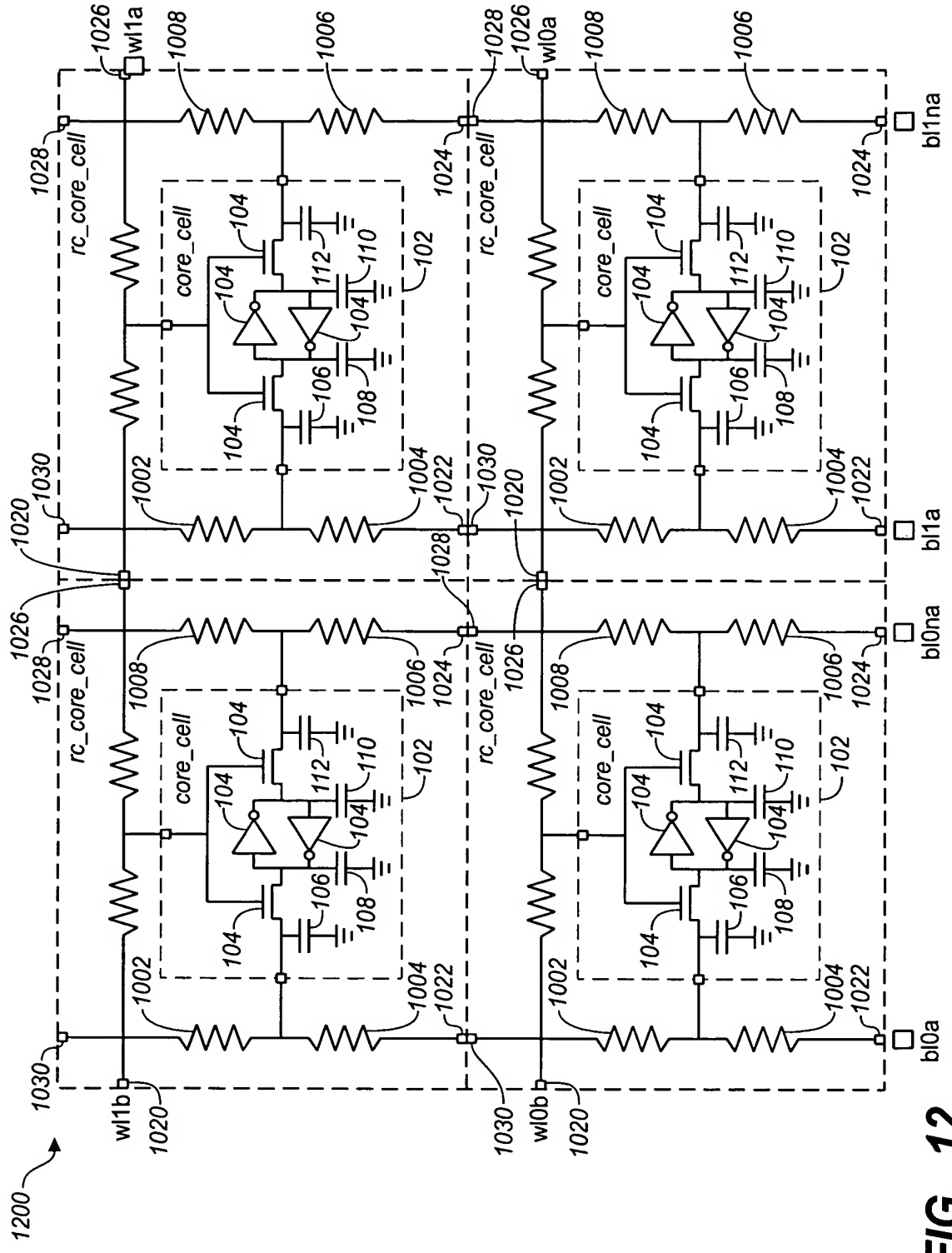
1200
wl1b
wl0b
wl1a
wl0a
bl0a
bl0na
bl1a
bl1na
rc_core_cell
core_cell
1002
1004
1006
1008
1020
1022
1024
1026
1028
1030
102
104
106
108
110
112

FIG._12

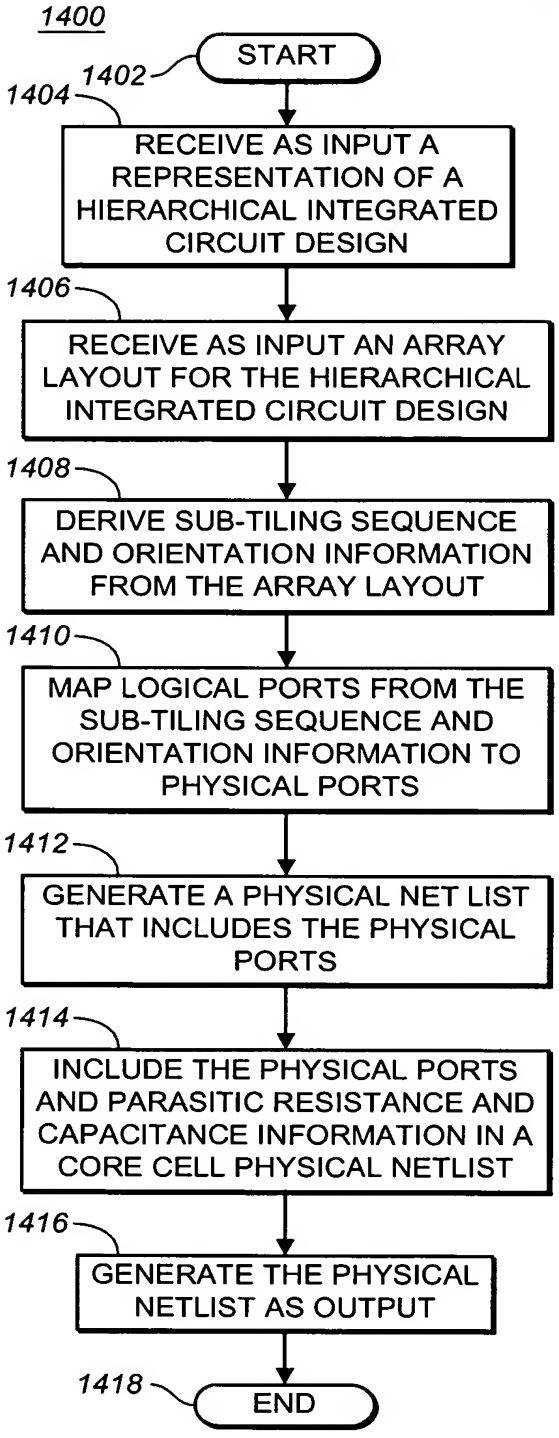
1400
START
1402
1404
RECEIVE AS INPUT A REPRESENTATION OF A HIERARCHICAL INTEGRATED CIRCUIT DESIGN
1406
RECEIVE AS INPUT AN ARRAY LAYOUT FOR THE HIERARCHICAL INTEGRATED CIRCUIT DESIGN
1408
DERIVE SUB-TILING SEQUENCE AND ORIENTATION INFORMATION FROM THE ARRAY LAYOUT
1410
MAP LOGICAL PORTS FROM THE SUB-TILING SEQUENCE AND ORIENTATION INFORMATION TO PHYSICAL PORTS
1412
GENERATE A PHYSICAL NET LIST THAT INCLUDES THE PHYSICAL PORTS
1414
INCLUDE THE PHYSICAL PORTS AND PARASITIC RESISTANCE AND CAPACITANCE INFORMATION IN A CORE CELL PHYSICAL NETLIST
1416
GENERATE THE PHYSICAL NETLIST AS OUTPUT
1418
END

FIG._14

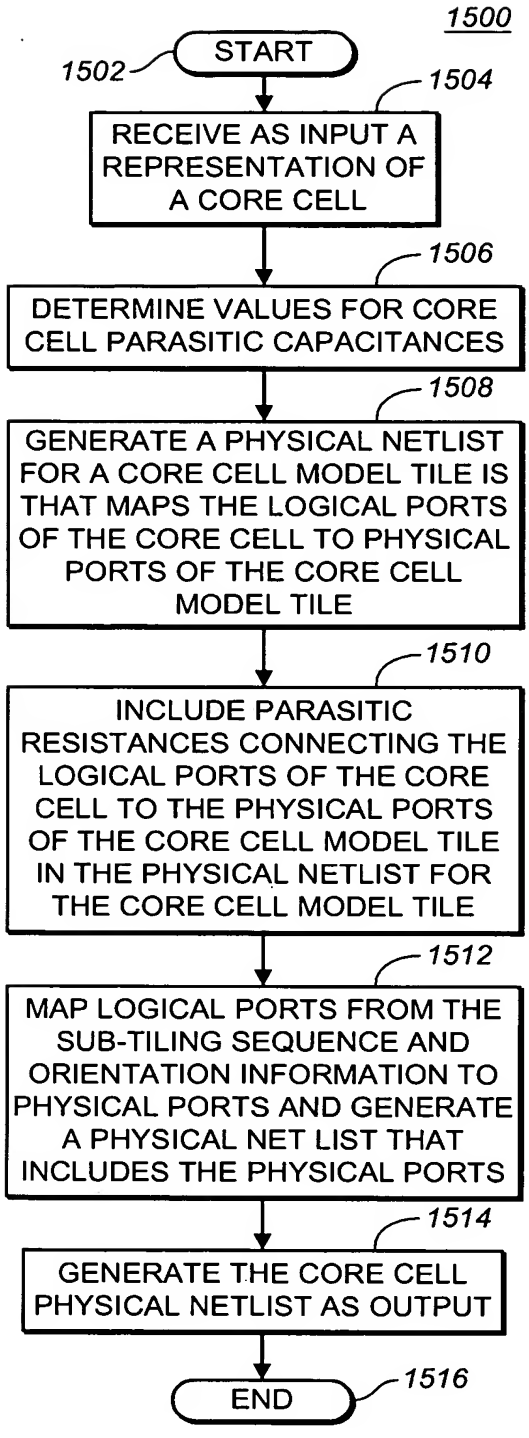
1500
START
1502
1504
RECEIVE AS INPUT A REPRESENTATION OF A CORE CELL
1506
DETERMINE VALUES FOR CORE CELL PARASITIC CAPACITANCES
1508
GENERATE A PHYSICAL NETLIST FOR A CORE CELL MODEL TILE IS THAT MAPS THE LOGICAL PORTS OF THE CORE CELL TO PHYSICAL PORTS OF THE CORE CELL MODEL TILE
1510
INCLUDE PARASITIC RESISTANCES CONNECTING THE LOGICAL PORTS OF THE CORE CELL TO THE PHYSICAL PORTS OF THE CORE CELL MODEL TILE IN THE PHYSICAL NETLIST FOR THE CORE CELL MODEL TILE
1512
MAP LOGICAL PORTS FROM THE SUB-TILING SEQUENCE AND ORIENTATION INFORMATION TO PHYSICAL PORTS AND GENERATE A PHYSICAL NET LIST THAT INCLUDES THE PHYSICAL PORTS
1514
GENERATE THE CORE CELL PHYSICAL NETLIST AS OUTPUT
1516
END

FIG._15